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(54) **Semiconductor device with aligned oxide apertures and contact to an intervening layer**

Halbleitervorrichtung mit ausgerichteten Oxidöffnungen und Kontaktierung einer Zwischenschicht

Dispositif semi-conducteur avec ouvertures d'oxyde alignées et mise en contact d'une couche intermédiaire

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- **LIM D H ET AL: "SEALING OF ALAS AGAINST WET OXIDATION AND ITS USE IN THE FABRICATION OF VERTICAL-VAVITY SURFACE-EMITTING LASERS" APPLIED PHYSICS LETTERS,US,AMERICAN INSTITUTE OF PHYSICS. NEW YORK, vol. 71, no. 4, page 1915-1917 XP000725826 ISSN: 0003-6951**
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Description

[0001] This invention relates to a semiconductor device including a long-wavelength vertical cavity surface emitting laser (VCSEL) that is optically pumped by an integrated short-wavelength VCSEL, and more particularly to a process for use in fabrication of such a semiconductor device.

[0002] A vertical cavity surface emitting laser (VCSEL) is a semiconductor laser including a semiconductor layer of optically active material, such as gallium arsenide or indium phosphide. The optically active material is sandwiched between mirror stacks formed of highly-reflective layers of metallic material, dielectric material, or epitaxially-grown semiconductor material. Conventionally, one of the mirror stacks is partially reflective so as to pass a portion of the coherent light which builds up in a resonating cavity formed by the mirror stacks sandwiching the active layer.

[0003] Lasing structures require optical confinement in the resonating cavity and carrier confinement in the active region to achieve efficient conversion of pumping electrons into stimulated photons through population inversion. The standing wave of reflected optical energy in the resonating cavity has a characteristic cross-section giving rise to an optical mode. A desirable optical mode is the single fundamental transverse mode, for example, the HE_{11} mode of a cylindrical waveguide. A single mode signal from a VCSEL is easily coupled into an optical fibre, has low divergence, and is inherently single frequency in operation.

[0004] In order to reach the threshold for lasing, the total gain of a VCSEL must equal the total loss of the VCSEL. Unfortunately, due to the compact nature of VCSELs, the amount of gain media is limited. For efficient VCSELs, at least one of the two required mirrors must have a reflectivity greater than approximately 99.5%. It is more difficult to meet this requirement in long-wavelength VCSELs than in short-wavelength VCSELs because such high reflectivity mirrors are difficult to grow in the same epitaxial step as the long-wavelength active region. Because epitaxially-grown mirror stacks often do not enable sufficiently high reflectivity, some VCSELs are formed by wafer fusing the top and bottom mirror stacks to the active region.

[0005] Wafer fusion is a process by which materials of different lattice constant are atomically joined by applying pressure and heat to create a real physical bond. Thus, wafer fusion of one or both of the mirror stacks to the active region is used to increase the reflectivity provided by either or both of the mirrors to compensate for the small amount of gain media so that the lasing threshold can be reached and maintained.

[0006] An important requirement for low-threshold, high-efficiency VCSEL operation is a lateral refractive index variation or index guiding mechanism that introduces low optical loss for the VCSEL. Lateral oxidation of AlGaAs has been used for refractive index guiding to make high-efficiency VCSELs. In such a lateral oxidation technique, a mesa is etched into the top surface of the VCSEL wafer, and the exposed sidewalls of an AlGaAs layer are exposed to water vapour. Water vapour exposure causes conversion of the AlGaAs to $AlGaO_x$, some distance in from the sidewall toward the central vertical axis, depending on the duration of the oxidation. This introduces a lateral refractive index variation, creating a low-loss optical waveguide if the $AlGaO_x$ layer is sufficiently thin.

[0007] A long-wavelength VCSEL can be optically coupled to and optically pumped by a shorter wavelength, electrically pumped VCSEL. US Patent No. 5,513,204 to Jayaraman entitled "LONG WAVELENGTH, VERTICAL CAVITY SURFACE EMITTING LASER WITH VERTICALLY INTEGRATED OPTICAL PUMP" describes an example of a short-wavelength VCSEL optically pumping a long-wavelength VCSEL.

[0008] Two key requirements for manufacturing a long-wavelength VCSEL optically pumped by an integrated short-wavelength VCSEL are precise alignment of the optical mode of the two VCSELs over a wafer scale, combined with electrical contact with both a p-doped and an n-doped layer of the short-wavelength VCSEL.

[0009] This has been accomplished in the past using patterned wafer fusion to define the optical mode of the long-wavelength VCSEL, while using oxidation to define the optical mode of the short-wavelength pump VCSEL. This necessitates the difficult task of precise, sub-micron infrared photolithography over a full wafer.

[0010] The invention provides a process for use in fabrication of a semiconductor device. In the process, a short-wavelength vertical cavity surface emitting laser (VCSEL) is epitaxially grown on and integrated with a top long-wavelength distributed Bragg reflector. A long-wavelength active region is wafer fused to a bottom long-wavelength distributed Bragg reflector. The top long-wavelength distributed Bragg reflector is wafer fused to the long-wavelength active region, making a long-wavelength VCSEL beneath the short-wavelength VCSEL. The short-wavelength VCSEL includes a top oxidation layer of AlGaAs. The long-wavelength VCSEL includes a bottom oxidation layer of AlGaAs. An n-doped contact layer is interposed between the top oxidation layer of AlGaAs and the bottom oxidation layer of AlGaAs. P-type metal is deposited on a top surface of the short-wavelength VCSEL to make a p-contact of the semiconductor device. A mesa is etched in the short-wavelength VCSEL down to the n-doped contact layer, thereby forming a field around the mesa. N-type metal is deposited in the field to make an n-contact of the semiconductor device. One or more holes are patterned on top of the mesa, radially outward from the p-type metal deposit, in the shape of a non-continuous ring around the p-type metal deposit. The patterned one or more holes are etched from the top of the mesa downward through both the top oxidation layer of AlGaAs and the

bottom oxidation layer of AlGaAs, and the one or more etched holes are oxidized in a single step, thereby forming a top oxide aperture in the short-wavelength VCSEL and a bottom oxide aperture in the long-wavelength VCSEL. The top oxide aperture and the bottom oxide aperture are collinear along the central vertical axis of the semiconductor device.

[0011] According to an exemplary embodiment of the invention, the fabricated semiconductor includes a short wave-length vertical cavity surface emitting laser (VCSEL). The short-wavelength VCSEL includes a top oxidation layer. A long-wavelength VCSEL is monolithically integrated with and optically pumped by the short-wavelength VCSEL. The long-wavelength VCSEL includes a bottom oxidation layer. A top oxide aperture is defined by the top oxidation layer, and a bottom oxide aperture is defined by the bottom oxidation layer. An n-doped contact layer is interposed between the top oxidation layer and the bottom oxidation layer. The semiconductor device presents a central vertical axis, and the top oxide aperture and the bottom oxide aperture are each centered about the central vertical axis in respective planes that are both perpendicular to the central vertical axis.

[0012] Other features and advantages of the invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawing, which illustrate, by way of example, the features of the invention.

[0013] Fabricated semiconductor devices and methods of fabrication are defined in Claims 1-28.

[0014] In the drawings:

FIG. 1 is a top plan view of a semiconductor device according to the principles of the invention;

FIG. 2 is a cross-sectional view taken along the line A-A' in FIG. 1 (hatching has been removed to aid clarity); and

FIG. 3 is a process flow diagram for describing fabrication of a semiconductor device according to the principles of the invention.

[0015] In this description, "top" or "upper" are relative terms referring to regions of the semiconductor device away from the substrate, and the "bottom" and "lower" mean toward the substrate.

[0016] As shown in the drawings for purposes of illustration, a long-wavelength vertical cavity surface emitting laser (VCSEL) is optically coupled to and optically pumped by a short-wavelength VCSEL in a monolithic integrated semiconductor device. Semiconductor devices in accordance with the principles of the invention can be manufactured in groups or arrays in a wafer-scale integrated circuit system.

[0017] Successful manufacturing of the monolithic integrated semiconductor device requires the ability to precisely align the optical mode of the two VCSELs over a wafer scale and make electrical contact to both p-material and n-material layers of the short-wavelength VCSEL.

[0018] Previous attempts to use patterned wafer fusion to define the optical mode of the long-wavelength VCSEL, and oxidation to define the optical mode of the short-wavelength VCSEL pump, often require precise, sub-micron infrared photolithography over a full wafer, which is difficult.

[0019] A better technique than using patterned wafer fusion to define the optical mode of the long-wavelength VCSEL along with oxidation to define the optical mode of the short-wavelength pump is to use a self-aligned process, which does not require manual alignment during processing. In a self-aligned process, a deep mesa is etched past an oxidation layer in each of the two VCSELs. Then the two oxidation layers are simultaneously oxidised. The two oxide apertures in the two oxidation layers, respectively, that result are self-aligned, but there is no way to make electrical contact to a layer between the oxidation layers.

[0020] To overcome the aforementioned and other shortcomings the invention provides a process for use in fabricating a monolithically integrated semiconductor device that includes a long-wavelength VCSEL optically coupled to and optically pumped by a short-wavelength VCSEL. In the fabricated semiconductor device there are two vertically-aligned oxide apertures in the two oxidation layers, respectively, and electrical contact is made to a layer between the two oxidation layers.

[0021] The process is described with reference to FIGS. 1 and 2, where a composite-layer semiconductor device has been fabricated from a wafer that includes a plurality of layers. FIG. 1 illustrates a top view of the fabricated monolithically-integrated semiconductor device. With reference to FIG. 1 an n-type metal contact 10 has been deposited on a contact layer of the fabricated semiconductor device. The n-type metal contact 10 surrounds a mesa 12 that has a cloverleaf-shaped cross-sectional configuration. A p-type metal contact 14 has been deposited on the cloverleaf-shaped mesa 12. A set 16 of four deep oxidation holes are defined by the cloverleaf-shaped mesa 12 and extend upward and downward inside the mesa 12. The four deep oxidation holes 16 surround the vertically-aligned top oxide aperture 18 and bottom oxide aperture (not shown in FIG. 1) in the monolithic integrated circuit.

[0022] FIG. 2 illustrates a cross-sectional view taken along the line A-A' in FIG. 1. With reference to FIG. 2 the plurality of layers in the fabricated monolithic integrated semiconductor device includes a bottom 1300 nm mirror 22, a 1300 nm active region 24 disposed above the bottom 1300 nm mirror 22, and a top 1300 nm mirror 26 disposed above the 1300 nm active region 24, where the top 1300 nm mirror 26 includes a bottom oxidation layer 28 that defines the bottom oxide aperture 30 within the bottom oxidation layer 28. The bottom oxidation layer 28 corresponds to the 1300 nm active region 24.

[0023] The plurality of layers in the fabricated semiconductor device includes an n-doped bottom 850 nm mirror 34. The n-doped bottom 850 nm mirror 34 is epitaxially grown above the top 1300 nm mirror 26, integrated with the top 1300 nm mirror 26. The bottom 850 nm mirror 34 includes the contact layer 36 of the semiconductor device. The n-type metal contact 10 is applied to the n-doped contact layer 36 and partially surrounds the cloverleaf-shaped mesa 12. The top oxidation layer 38 defines the top oxide aperture 18 and is located above the contact layer 36. The fabricated multi-layer semiconductor device includes an 850 nm active region (not numbered in FIG. 2) disposed above the bottom 850 nm mirror 34, a p-doped top 850 nm mirror 42 disposed above the 850 nm active region.

[0024] During fabrication of the semiconductor device in accordance with the principles of the invention, a shallow mesa 12 is etched in the semiconductor wafer down to the contact layer 36 of the n-doped bottom 850 nm mirror 34 that is to be electrically contacted. The exposed area of the contact layer 36 presents a field partially circumscribing the etched mesa 12. The contact layer 36 is located between the top oxidation layer 38 and the bottom oxidation layer 28.

[0025] The deep oxidation holes 16 (FIG. 1) are etched from the top of the mesa 12 downward through the mesa 12 beyond both the top oxidation layer 38, which is within the short-wavelength VCSEL 44, and the bottom oxidation layer 28, which is within the long-wavelength VCSEL 46. Four deep oxidation holes 16 are illustrated in the top plan view of FIG. 1. In the sectional view of Fig. 2, two of the four deep oxidation holes are illustrated.

[0026] The p-type metal contact 14 is applied to the top of the p-doped top 850 nm mirror 42 of the short-wavelength VCSEL 44. The n-type metal contact 10 is applied on the field of the contact layer 36.

[0027] With reference to FIG. 2, current can move in the finished monolithic integrated circuit in a path from the n-type metal contact 10 to the contacting region, in the cloverleaf-shaped mesa structure 12 between the deep oxidation holes, through the top oxide aperture 18 to the p-type metal contact 14.

[0028] Simultaneous oxidation of the top oxide aperture 18 and the bottom oxide aperture 30 during fabrication of the monolithic semiconductor device according to the principles of the invention produces an alignment of the optical mode of the long-wavelength VCSEL 46 with the optical mode of the short-wavelength VCSEL 44 in the monolithic semiconductor device.

[0029] The bottom oxide aperture 30 defines the optical mode of the long-wavelength VCSEL 46. The top oxide aperture 18 defines the optical mode of the short-wavelength VCSEL 44 and defines, at least in part, the electric current path in the short-wavelength VCSEL 44.

[0030] Multiple vertically-aligned oxide apertures corresponding to multiple active regions in epitaxially grown structures can be achieved as taught herein. Referring to FIG. 2, each oxide aperture 18, 30 is disposed in the plane of its respective oxidation layer 38, 28. Each centre line that is normal to the plane in which each oxide aperture is disposed and that passes through the centre of each oxide aperture is substantially collinear with the other centre line(s) in accordance with the principles of the invention. Importantly, the centre line of each oxide aperture is collinear with the centre line(s) of the other oxide aperture(s) along a common central vertical axis 48 of the semiconductor device.

[0031] In the process of fabricating the semiconductor device, each vertically-aligned oxide aperture is formed by converting a semiconductor layer to an insulating, low-dieiectric-constant oxide layer through the process of wet oxidation. The resulting oxide apertures are caused to be aligned by etching a hole, or multiple holes, through all oxidation layers and defining the etch mask for this hole, or these holes, in a single alignment step (which is typically a photolithography step). The etch is followed by a single oxidation step which oxidizes all the layers simultaneously.

[0032] Precise alignment of the optical modes of the electrically pumped shorter wavelength VCSEL and the longer wavelength VCSEL that is optically pumped by the shorter wavelength VCSEL is an important aspect of the manufacturing optically pumped long-wavelength structures. According to previous practice, to align the optical modes of the electrically pumped VCSEL and the longer wavelength VCSEL that is optically pumped, patterned wafer fusion was used to define the long-wavelength aperture and lateral oxidation was used to define the short-wavelength aperture; and then such oxide aperture and such patterned fusion aperture were manually aligned using infrared photolithography. This is a difficult and time-consuming process and the alignment is not always satisfactory.

[0033] One better way to align the apertures of the two VCSELs is to simultaneously oxidise an oxidation layer in each VCSEL to create an aperture in each oxidation layer. The apertures generated after selective oxidation are automatically aligned if an etched hole, or multiple holes, traverses the oxidation layers of the 850 nm short-wavelength pump VCSEL and the 1300 nm long-wavelength VCSEL.

[0034] Because the etched feature (i.e. the set of deep oxidation holes) is not continuous around the entire circumference of the aperture, a current path exists from p-metal radially inward of the etched holes on top of the structure to n-metal radially outward of the etched holes in an n-layer (i.e. the contact layer) between the two oxidation layers. Using the invented process, one can, with repeatability, create vertically-aligned apertures within the 850 nm short-wavelength pump VCSEL and the 1300 nm long-wavelength VCSEL and still electrically contact both p-material and n-material layers of the 850 nm short-wavelength pump VCSEL.

[0035] The process of etching the deep hole, or holes, can be controlled according to the principles of the in-

vention to engineer a difference between the size of the top oxide aperture and the size of the bottom oxide aperture. For example, using the invented process one can intentionally introduce a taper to the side-wall allowing the top of the hole (or holes) to be wider than the bottom of the hole (or holes). When such a taper is introduced, if the top oxide aperture and the bottom oxide aperture are collinear along the central vertical axis of the monolithic integrated semiconductor device, and if the top oxide aperture and the bottom oxide aperture are located in planes that are perpendicular to the central vertical axis, then the radius or size of the bottom oxide aperture measured from the central vertical axis is greater than the radius or size of the top oxide aperture measured from the central vertical axis. In this case, the selective oxidation of identical oxidation layers renders the bottom aperture larger than the top.

[0036] Using the invented process one can also engineer the oxidation layers, and the apertures defined within the oxidation layers, by controlling the aluminium composition of the AlGaAs, the thickness of the layers of AlGaAs, the grade thickness, the doping concentration of the oxidation layers, or combinations of such fabrications parameters, or other related parameters. The resulting apertures will still be aligned, but their sizes will no longer be the same.

[0037] Also, the number, shape and placement of the holes can be controlled in the invented process to engineer a specific aperture shape.

[0038] A specific application of the invention is used in the manufacture of optically pumped long-wavelength VCSELs. The optically pumped structure includes two monolithically-integrated VCSELs. The top VCSEL of the two is electrically pumped to emit laser light at a shorter wavelength. The shorter wavelength laser light that is emitted by the top VCSEL stimulates the bottom VCSEL to emit laser light at a longer wavelength.

[0039] FIG. 3 is a process flow diagram for describing fabrication of a semiconductor device in accordance with the principles of the invention. In order to construct a composite-layer semiconductor device in accordance with the principles of the invention, a structure that includes two or more oxidation layers corresponding to two or more active regions is epitaxially grown. Referring to FIG. 3 a specific example of this structure can be made by growing an 850 nm pump laser with an integrated top 1300 nm Distributed Bragg Reflector (DBR) in step 50. A 1300 nm active region is wafer fused to a bottom 1300 nm DBR in step 52. The top 1300 nm DBR is wafer fused to the 1300 nm active region to create a structure suitable for building an optically pumped VCSEL in step 54.

[0040] The 850 nm pump VCSEL and integrated top 1300 nm DBR each have a high-percentage AlGaAs layer which can be oxidized selectively with respect to the surrounding epitaxial layers. The n-doped, n-material contact layer of the 850 nm pump VCSEL is situated between the two high-percentage AlGaAs layers. At this stage of the wafer-scale fabrication process, the integrated semiconductor device includes an 850 nm VCSEL optically coupled,to an integrated 1300 nm VCSEL beneath the 850 nm VCSEL.

[0041] After epitaxially growing the wafer and performing the necessary wafer fusion steps that result in the 850 nm VCSEL optically coupled to the integrated 1300 nm VCSEL, p-metal is deposited on the top surface of the 850 nm pump VCSEL in the wafer to make what will become the top p-type contact of the integrated semiconductor device in step 56.

[0042] Then, a mesa, which includes the p-metal deposit on its top surface, is etched in the wafer down to the n-doped contact layer of the 850 nm VCSEL in step 58. This forms a field at least partially circumscribing the etched mesa. The etching can include, for example, a dry plasma based etch or a wet chemical etch. After the mesa etching is completed, n-contact metal is deposited in the etched field in step 60.

[0043] Both the p-type metal contact and the n-type metal contact are then alloyed in a rapid thermal annealing process in step 62. There are now completed electrical contacting layers for electrically pumping the 850 nm pump VCSEL of the monolithic integrated circuit.

[0044] The terms "p" and "n" as used herein to identify metal-type and doping may be interchanged within the scope of the present invention.

[0045] In step 64 the device is then coated with SiNx, which serves to protect both p-type and n-type metal contacts during a subsequent oxidation step, and aids in production of a reproducible vertical sidewall during the subsequent hole etch down through the mesa.

[0046] After deposition of the SiNx, one or more holes to be etched are patterned on top of the mesa in step 66. The patterned holes are radially outward of the p-metal deposit, as measured from the central vertical axis. These holes are etched from the top of the mesa down through the SiNx, into the wafer past both the top AlGaAs oxidation layer and the bottom AlGaAs oxidation layer in step 68. The etched holes form a non-continuous ring around the p-metal deposit.

[0047] After the holes are etched, a single oxidation step is performed in step 70, which creates in this specific embodiment two vertically-aligned oxide apertures. The bottom oxide aperture confines the optical mode of the 1300 nm VCSEL radially inward toward the central vertical axis and along the central vertical axis. Etching past both the top oxidation layer and the bottom oxidation layer in the same alignment step as taught herein ensures that the centres of the two apertures, after being formed through selective oxidation, will be aligned.

[0048] Following the single oxidation step, the SiNx coating is removed by etching in step 72. A thin SiNx coating that serves as a 1300 nm anti-reflection coating is deposited over the device in step 74. The anti-reflection coating is patterned and etched to open access to the 850 nm p-type and n-type electrical contacts in step 76. The anti-reflection coating is maintained over the ap-

erture of the optically pumped device. The device is now complete.

[0049] Each monolithically-integrated. multi-layer semiconductor device produced by the foregoing process includes a long-wavelength VCSEL optically coupled to and optically pumped by a short-wavelength VCSEL, which in the preferred embodiment is disposed above the long-wavelength VCSEL. It is contemplated that arrays of semiconductor devices can be produced on a wafer scale using the invented process.

[0050] The layers of the fabricated semiconductor device include a first oxidation layer, which is part of the short-wavelength VCSEL, and a second oxidation layer, which is part of the long-wavelength VCSEL. A first oxide aperture is defined by the first oxidation layer and a second oxide aperture is defined by the second oxidation layer. The first oxide aperture and the second oxide aperture are vertically aligned with respect to a central vertical axis. An n-type metal contact is applied to a contact layer within the semiconductor device that is interposed between the first oxidation layer and the second oxidation layer.

[0051] While several particular forms of the invention have been illustrated and described, it will also be apparent that various modifications can be made without departing from the scope of the invention.

Claims

1. A process for use in fabrication of a semiconductor device,

the fabricated semiconductor device comprising a top oxide aperture (18) defined by a top oxidation layer (38), a bottom oxide aperture (30) defined by a bottom oxidation layer (28), and a contact layer (36) adapted for electrical contact and disposed between the top oxidation layer (38) and the bottom oxidation layer (28),

wherein the fabricated semiconductor device presents a central vertical axis (48), and the top oxide aperture (18) and the bottom oxide aperture (30) are collinear along the central vertical axis (48), wherein the semiconductor devices includes a long-wavelength vertical cavity surface emitting laser (VCSEL) (46) optically pumped by a short-wavelength VCSEL (44) having a wavelength less than said long-wavelength VCSEL (46);

wherein the top oxidation layer (38) is within the short-wavelength VCSEL (44), and

wherein the bottom oxidation layer (28) is within the long-wavelength VCSEL (46),

the process comprising the steps of:

etching past the top oxidation layer (38) and stopping in the contact layer (36),

etching one or more holes traversing the top oxidation layer (38) and the bottom oxidation layer (28), and

simultaneously oxidizing both the top oxidation layer (38) and the bottom oxidation layer (28) laterally from inside said holes.

2. A process as claimed in claim 1, further comprising the step of:

controlling the size of the top oxide aperture (18) relative to the size of the bottom oxide aperture (30).

3. A process as claimed in claim 2, further comprising the step of:

controlling the doping concentration of the top oxidation layer (38) and the bottom oxidation layer (28).

4. A process as claimed in claim 2, further comprising the step of:

controlling the neighboring grade profile for the top oxidation layer (38) and the bottom oxidation layer (28).

5. A process as claimed in claim 2, further comprising the step of:

controlling the layer thickness of the top oxidation layer (38) and the bottom oxidation layer (28).

6. A process as claimed in claim 2, further comprising the step of:

controlling layer composition in the top oxidation layer (38) relative to the layer composition in the bottom oxidation layer (28).

7. A process as claimed in any preceding claim, wherein

in the fabricated semiconductor device, the size of the top oxide aperture (18) is different from the size of the bottom oxide aperture (30).

8. A process as claimed in any preceding claim, wherein:

each of the top oxidation layer (38) and the bottom oxidation layer (28) corresponds, respectively, to an active region.

9. A process for use in fabrication of a semiconductor device that has a central vertical axis (48), comprising the steps of:

epitaxially growing a short-wavelength vertical

cavity surface emitting laser (VCSEL) (44) integrated with a top long-wavelength distributed Bragg reflector,

wafer fusing a long-wavelength active region to a bottom long-wavelength distributed Bragg reflector,

wafer fusing the top long-wavelength distributed Bragg reflector to the long-wavelength active region, making a long-wavelength VCSEL (46) beneath the short-wavelength VCSEL (44),

wherein the short-wavelength VCSEL (44) includes a top oxidation layer (38) of AlGaAs,

the long-wavelength VCSEL (46) includes a bottom oxidation layer (28) of AlGaAs,

a first contact layer (14) is disposed above said top oxidation layer (38) of AlGaAs, and

a second contact layer (36) is interposed between the top oxidation layer (38) of AlGaAs and the bottom oxidation layer (28) of AlGaAs,

depositing a first metal on said first contact layer (14) to make a first contact of the semiconductor device,

etching a mesa (12) in the short-wavelength VCSEL (44) down to said second contact layer, thereby forming a field around the mesa (12),

depositing a second metal in the field to make a second contact of the semiconductor device,

patterning one or more holes on top of the mesa (12), in the shape of a non-continuous ring,

etching the patterned one or more holes from the top of the mesa (12) downward through both the top oxidation layer (38) of AlGaAs and the bottom oxidation layer (28) of AlGaAs, and

oxidizing the one or more etched holes in a single step, thereby forming a top oxide aperture (18) in the short-wavelength VCSEL (44) and a bottom oxide aperture (30) in the long-wavelength VCSEL (46),

wherein the top oxide aperture (18) and the bottom oxide aperture (30) are collinear along the central vertical axis (48).

10. A process as claimed in claim 9, wherein:

each of the top oxidation layer (38) and the bottom oxidation layer (28) can be oxidized selectively with respect to the surrounding epitaxial layers.

11. A process as claimed in claim 9 or 10, wherein:

the etching of the mesa (12) in the short-wavelength VCSEL (44) uses a dry plasma based etch.

12. A process as claimed in claim 9 or 10, wherein:

the etching of the mesa (12) in the short-wavelength VCSEL (44) uses a wet chemical etch.

13. A process as claimed in any of claims 9 to 12, wherein:

the etched mesa (12) includes the first metal on the top surface of the short-wavelength VCSEL (44).

14. A process as claimed in any of claims 9 to 13, further comprising the step of:

alloying the first contact and the second contact using a rapid thermal annealing process.

15. A process as claimed in any preceding claim, wherein:

the etching of the patterned holes through both the top oxidation layer (38) and the bottom oxidation layer (28) is performed in a single step.

16. A process as claimed in any preceding claim, further comprising the steps of:

before the patterning of the one or move holes, depositing a coat of SiNx over the device.

17. A process as claimed in claim 16, further comprising the step of:

removing the coat of SiNx,

depositing a long-wavelength anti-reflection coating over the device,

patterning the anti-reflection coating, and

etching the anti-reflection coating to open access to the first contact and the second contact.

18. A process as claimed in any preceding claim, wherein:

the top oxide aperture (18) and the bottom oxide aperture (30) confine the optical mode of the semiconductor device.

19. A process as claimed in any of claims 9 to 18 comprising:

etching past the top oxidation layer (38) and stopping in the contact layer (36).

20. A semiconductor device comprising:

a top oxide aperture (18) defined in a top oxidation layer (38) above a bottom oxide aperture (30) defined in a bottom oxidation layer (28),

wherein the top oxide aperture (18) and the bottom oxide aperture (30) are collinear along a central vertical axis (48),

an electrical contact to a contact layer (36) between the top oxidation layer (38) and the bottom oxidation layer (28),

wherein the top oxide aperture (18) is part of a short-wavelength vertical cavity surface emitting laser (VCSEL) (44),

the bottom oxide aperture (30) is part of a long-wavelength VCSEL (46), and

the short-wavelength VCSEL (44) optically pumps the long-wavelength VCSEL (46).

21. A semiconductor device as claimed in claim 20, wherein the long-wavelength VCSEL (46) includes:

a bottom mirror (22),
an active region wafer (24) fused to the bottom mirror (22), and
a top mirror wafer (26) fused to the active region (24).

22. A semiconductor device as claimed in claims 20 or 21, wherein:

the long-wavelength VCSEL (46) emits laser light having a wavelength in a range from about 1250nm to about 1650nm.

23. A semiconductor device as claimed in any of claims 20 to 22, wherein:

the top oxide aperture (18) and the bottom oxide aperture (30) are each centered about the central vertical axis (48) in respective planes that are both perpendicular to the central vertical axis (48).

24. A semiconductor device as claimed in any of claims 20 to 23, wherein:

the short-wavelength VCSEL (44) is electrically pumped and includes a p-doped top mirror (42).

25. A semiconductor device as claimed in claim 24, wherein:

current is confined to flow through a current path that includes the top mirror (42), the top oxide aperture (18) and the contact layer (36).

26. A semiconductor device as claimed in any of claims 20 to 25, wherein:

the short-wavelength VCSEL (44) emits laser light having a wavelength in a range from about 700nm to about 1050nm.

27. A semiconductor device as claimed in any of claims 20 to 26, wherein:

optical energy is guided by the top oxide aperture (18) and the bottom oxide aperture (30).

28. A semiconductor device as claimed in any of claims 20 to 27, wherein:

the top oxidation layer (38) and the bottom oxidation layer (28) form a lateral refractive index guide.

Patentansprüche

1. Verfahren zur Verwendung bei der Fertigung eines Halbleiterbauelements,
wobei das hergestellte Halbleiterbauelement eine obere Oxidöffnung (18), die durch eine obere Oxidationsschicht (38) definiert ist, eine in einer unteren Oxidationsschicht (28) definierte untere Oxidöffnung (30) und eine Kontaktschicht (36) zur elektrischen Kontaktgabe zwischen der oberen Oxidationsschicht (38) und der unteren Oxidationsschicht (28) aufweist,
wobei das hergestellte Halbleiterbauelement eine zentrale vertikale Achse (48) aufweist, entlang der die obere Oxidöffnung (18) und die untere Oxidöffnung (30) kollinear verlaufen, wobei das Halbleiterbauelement einen oberflächenemittierenden Laser mit vertikalem Hohlraum (VCSEL) für lange Wellenlängen (46) enthält, der optisch gepumpt wird von einem Kurzwellenlängen-VCSEL (44), dessen Wellenlänge kleiner ist als die des Langwellenlängen-VCSEL (46);
wobei die obere Oxidationsschicht (38) sich innerhalb des Kurzwellenlängen-VCSEL (44) befindet, und
wobei die untere Oxidationsschicht (28) sich innerhalb des Langwellenlängen-VCSEL (46) befindet,
wobei das Verfahren folgende Schritte beinhaltet:

Ätzen an der oberen Oxidationsschicht (38) vorbei und Anhalten in der Kontaktschicht (36),

Ätzen von einem oder mehreren Löchern, die die obere Oxidationsschicht (38) und die untere Oxidationsschicht (28) durchsetzen, und

gleichzeitiges Oxidieren sowohl der oberen Oxidationsschicht (38) als auch der unteren Schicht (28) in seitlicher Richtung ausgehend von dem Inneren der Löcher.

2. Verfahren nach Anspruch 1, weiterhin umfassend:

Steuern der Größe der oberen Oxidöffnung

(18) relativ zur Größe der unteren Oxidöffnung (30).

3. Verfahren nach Anspruch 2, weiterhin umfassend den Schritt:

Steuern der Dotierstoffkonzentration der oberen Oxidationsschicht (38) und der unteren Oxidationsschicht (28).

4. Verfahren nach Anspruch 2, weiterhin umfassend den Schritt:

Steuern des Nachbar-Stufenprofils für die obere Oxidationsschicht (38) und die untere Oxidationsschicht (28).

5. Verfahren nach Anspruch 2, weiterhin umfassend den Schritt:

Steuern der Schichtdicke der oberen Oxidationsschicht (38) und der unteren Oxidationsschicht (28).

6. Verfahren nach Anspruch 2, weiterhin umfassend den Schritt:

Steuern der Schichtzusammensetzung in der oberen Oxidationsschicht (38) relativ zu der Schichtzusammensetzung in der unteren Oxidationsschicht (28).

7. Verfahren nach einem vorhergehenden Anspruch, bei dem innerhalb des gefertigten Halbleiterbauelements die Größe der oberen Oxidöffnung (18) verschieden ist von der Größe der unteren Oxidöffnung (30).

8. Verfahren nach einem vorhergehenden Anspruch, bei dem sowohl die obere Oxidationsschicht (38) als auch die untere Oxidationsschicht (28) einer aktiven Zone entspricht.

9. Verfahren zur Verwendung bei der Fertigung eines Halbleiterbauelements, das eine zentrale vertikale Achse (48) aufweist, umfassend folgende Schritte:

epitaktisches Wachsen-Lassen eines oberflächenemittierenden Lasers mit vertikalem Hohlraum (VCSEL) für kurze Wellenlängen (44), integriert mit einem oberen verteilten Langwellen-Bragg-Reflektor,

Wafer-Schmelzen einer aktiven Langwellen-Zone auf einen unteren verteilten Langwellen-Bragg - Reflektor,

Wafer-Schmelzen des oberen verteilten Langwellen-Bragg-Reflektors an die aktive Langweilen-Zone, so daß unterhalb des Kurzwellen-VCSEL (44) der Langwellen-VCSEL (46) gelangt,

wobei der Kurzwellen-VCSEL (44) eine obere Oxidationsschicht (38) aus AlGaAs enthält,
der Langwellen-VCSEL (46) eine untere Oxidationsschicht (28) aus AlGaAs enthält,
eine erste Kontaktschicht (14) oberhalb der oberen Oxidationsschicht (38) aus AlGaAs gebildet wird, und
eine zweite Kontaktschicht (36) zwischen der oberen Oxidationsschicht (38) aus AlGaAs und der unteren Oxidationsschicht (28) aus AlGaAs ausgebildet wird,
auf der ersten Kontaktschicht (14) ein erstes Metall niedergeschlagen wird, um einen ersten Kontakt des Halbleiterbauelements zu bilden,
in dem Kurzwellen-VCSEL (44) hinunter zu der zweiten Kontaktschicht ein Mesa (12) geätzt wird, um um den Mesa (12) herum ein Feld zu bilden,
in dem Feld ein zweites Metall niedergeschlagen wird, um einen zweiten Kontakt des Halbleiterbauelements zu bilden,
oben auf dem Mesa (12) in Form eines nicht durchgehenden Rings ein oder mehrere Löcher ausgebildet werden,
das eine oder die mehreren ausgebildeten Löcher von oberhalb des Mesa (12) her nach unten sowohl durch die obere Oxidationsschicht (38) aus AlGaAs als auch die untere Oxidationsschicht (28) aus AlGaAs geätzt wird/werden, und
das eine oder die mehreren geätzten Löcher in einem einzigen Schritt oxidiert werden, um dadurch in dem Kurzwellen-VCSEL (44) eine obere Oxidöffnung (18) zu bilden und in dem Langwellen-VCSEL (46) eine obere Oxidöffnung (30) auszubilden,
wobei die obere Oxidöffnung (18) und die untere Oxidöffnung (30) entlang der zentralen vertikalen Achse (48) kollinear sind.

10. Verfahren nach Anspruch 9, bei dem sowohl die obere Oxidationsschicht (38) als auch die untere Oxidationsschicht (28) selektiv bezüglich der umgebenden Epitaxieschichten oxidierbar sind.

11. Verfahren nach Anspruch 9 oder 10, bei dem das Ätzen des Mesas (12) in dem Kurzwellen-VCSEL (44) vom Trockenplasmaätzen Gebrauch macht.

12. Verfahren nach Anspruch 9 oder 10, bei dem das Ätzen des Mesas (12) in dem Kurzwellen-VCSEL (44) vom chemischen Naßätzen Gebrauch macht.

13. Verfahren nach einem der Ansprüche 9 bis 12, bei dem der geätzte Mesa (12) das erste Metall auf der Oberseite des Kurzwellen-VCSEL (44) aufweist.

14. Verfahren nach einem der Ansprüche 9 bis 13, weiterhin umfassend den Schritt:

Legieren des ersten Kontakts und des zweiten Kontakts unter Verwendung eines schnellen thermischen Glühverfahrens.

15. Verfahren nach einem vorhergehenden Anspruch, bei dem das Ätzen der als Muster gebildeten Löcher durch sowohl die obere Oxidationsschicht (38) als auch die untere Oxidationsschicht (28) in einem einzigen Schritt erfolgt.

16. Verfahren nach einem vorhergehenden Anspruch, weiterhin umfassend die Schritte:

vor der Ausbildung des einen oder der mehreren Löcher wird über das Bauelement ein Überzug aus SiNx gebildet.

17. Verfahren nach Anspruch 16, weiterhin umfassend die Schritte:

Beseitigen des Überzugs aus SiNx,

Niederschlagen einer Langwellen-Antireflexionsbeschichtung auf dem Bauelement,

Ausbilden eines Musters in der Antireflexionsbeschichtung, und

Ätzen der Antireflexionsbeschichtung zum Verschaffen von Zugang zu dem ersten Kontakt und dem zweiten Kontakt.

18. Verfahren nach einem vorhergehenden Anspruch, bei dem die obere Oxidöffnung (18) und die untere Oxidöffnung (30) den optischen Moden des Halbleiterbauelements eingrenzt.

19. Verfahren nach einem der Ansprüche 9 bis 18, umfassend das Ätzen an der oberen Oxidationsschicht (38) vorbei und Anhalten des Ätzvorgangs in der Kontaktschicht (36).

20. Halbleiterbauelement, umfassend:

eine obere Oxidöffnung (18), die in einer oberen Oxidationsschicht (38) oberhalb einer unteren Oxidöffnung (30) in einer unteren Oxidationsschicht (28) definiert ist,

wobei die obere Oxidöffnung (18) und die untere Oxidöffnung (30) entlang einer zentralen vertikalen Achse (48) kollinear sind,
einen elektrischen Kontakt zu einer Kontaktschicht (36) zwischen der oberen Oxidationsschicht (38) und der unteren Oxidationsschicht (28),

wobei die obere Oxidöffnung (18) Teil eines oberflächenemittierenden Lasers mit vertikalem Hohlraum (VCSEL) für kurze Wellenlängen (44) ist,
die untere Oxidöffnung (30) Teil eines Langwellen-VCSEL (46) ist, und
der Kurzwellen-VCSEL (44) den Langwellen-VCSEL (46) optisch pumpt.

21. Halbleiterbauelement nach Anspruch 20, bei dem der Langwellen-VCSEL (46) enthält:

einen unteren Spiegel (22),

einen aktiven Zonenwafer (24), der auf den unteren Spiegel (22) geschmolzen ist, und

einen oberen Spiegelwafer (26), der auf die aktive Zone (24) geschmolzen ist.

22. Halbleiterbauelement nach Anspruch 20 oder 21, bei dem der Langwellen-VCSEL (46) Laserlicht mit einer Wellenlänge im Bereich von etwa 1250 nm bis etwa 1650 nm emittiert.

23. Halbleiterbauelement nach einem der Ansprüche 20 bis 21, bei dem die obere Oxidöffnung (18) und die untere Oxidöffnung (30) jeweils bezüglich der mittleren vertikalen Achse (48) in jeweiligen Ebenen zentriert sind, die beide rechtwinklig zu der zentralen vertikalen Achse (48) verlaufen.

24. Halbleiterbauelement nach einem der Ansprüche 20 bis 23, bei dem der Kurzwellen-VCSEL (44) elektrisch gepumpt wird und einen p-dotierten oberen Spiegel (42) enthält.

25. Halbleiterbauelement nach Anspruch 24, bei dem der Strom so eingegrenzt wird, daß er durch einen Strompfad fließt, der den oberen Spiegel (42), die obere Oxidöffnung (18) und die Kontaktschicht (36) enthält.

26. Halbleiterbauelement nach einem der Ansprüche 20 bis 25, bei dem das Kurzwellen-VCSEL (44) Laserlicht mit einer Wellenlänge im Bereich von etwa 700 nm bis etwa 1050 nm emittiert.

27. Halbleiterbauelement nach einem der Ansprüche 20 bis 26, bei dem optische Energie von der oberen Oxidöffnung (18) und der unteren Oxidöffnung (30) geführt wird.

28. Halbleiterbauelement nach einem der Ansprüche 20 bis 27, bei dem die obere Oxidationsschicht (38) und die untere Oxidationsschicht (28) eine laterale Brechungsindex-Führung bilden.

Revendications

1. Procédé destiné à être utilisé dans la fabrication d'un dispositif semiconducteur,

le dispositif semiconducteur fabriqué comprenant une ouverture d'oxyde supérieure (18) définie par une couche d'oxydation supérieure (38), une ouverture d'oxyde inférieure (30) définie par une couche d'oxydation inférieure (28) et une couche de contact (36) adaptée pour un contact électrique et disposée entre la couche d'oxydation supérieure (38) et la couche d'oxydation inférieure (28),

dans lequel le dispositif semiconducteur fabriqué présente un axe vertical central (48) et l'ouverture d'oxyde supérieure (18) et l'ouverture d'oxyde inférieure (30) sont colinéaires le long de l'axe vertical central (48), dans lequel le dispositif semiconducteur comporte un laser à émission de surface à cavité verticale de grande longueur d'onde (VCSEL) (46) pompé optiquement par un VCSEL de courte longueur d'onde (44) ayant une longueur d'ondes inférieure audit VCSEL de grande longueur d'onde (46) ;

dans lequel la couche d'oxydation supérieure (38) est à l'intérieur du VCSEL de courte longueur d'onde (44), et

dans lequel la couche d'oxydation inférieure (28) est à l'intérieur du VCSEL de grande longueur d'onde (46),

le procédé comprenant les étapes consistant à :

effectuer une gravure au-delà de la couche d'oxydation supérieure (38) et s'arrêter dans la couche de contact (36),
graver un ou plusieurs trous traversant la couche d'oxydation supérieure (38) et la couche d'oxydation inférieure (28), et
oxyder simultanément à la fois la couche d'oxydation supérieure (38) et la couche d'oxydation inférieure (28) latéralement par rapport auxdits trous intérieurs.

2. Procédé selon la revendication 1, comprenant en outre l'étape consistant à :

commander la taille de l'ouverture d'oxyde supérieure (18) par rapport à la taille de l'ouverture d'oxyde inférieure (30).

3. Procédé selon la revendication 2, comprenant en outre l'étape consistant à :

commander la concentration de dopage de la couche d'oxydation supérieure (38) et de la couche d'oxydation inférieure (28).

4. Procédé selon la revendication 2, comprenant en outre l'étape consistant à :

commander le profil de niveau au voisinage de couche d'oxydation supérieure (38) et de la couche d'oxydation inférieure (28).

5. Procédé selon la revendication 2, comprenant en outre l'étape consistant à :

commander l'épaisseur de couche de la couche d'oxydation supérieure (38) et de la couche d'oxydation inférieure (28).

6. Procédé selon la revendication 2, comprenant en outre l'étape consistant à :

commander la composition de couche dans la couche d'oxydation supérieure (38) par rapport à la composition de couche dans la couche d'oxydation inférieure (28).

7. Procédé selon l'une quelconque des revendications précédentes, dans lequel

dans le dispositif semiconducteur fabriqué, la taille de l'ouverture d'oxyde supérieure (18) est différente de la taille de l'ouverture d'oxyde inférieure (30).

8. Procédé selon l'une quelconque des revendications précédentes, dans lequel :

chacune parmi la couche d'oxydation supérieure (38) et la couche d'oxydation inférieure (28) correspond respectivement à une région active.

9. Procédé destiné à être utilisé dans la fabrication d'un dispositif semiconducteur comportant un axe vertical central (48), comprenant les étapes consistant à :

faire croître de façon épitaxiale un laser à émission de surface à cavité verticale de courte longueur d'onde (VCSEL) (44) intégré avec un réflecteur de Bragg distribué supérieur de grande longueur d'onde,
effectuer une fusion de tranche d'une région active de grande longueur d'onde vers un réflecteur de Bragg distribué inférieur de grande longueur d'onde,
effectuer une fusion de tranche du réflecteur de Bragg distribué supérieur de grande longueur d'onde vers la région active de grande longueur d'onde, réalisant un VCSEL de grande longueur d'onde (46) au-dessous du VCSEL de courte longueur d'onde (44),

dans lequel le VCSEL de courte longueur

d'onde (44) comporte une couche d'oxydation supérieure (38) d'AlGaAs,

le VCSEL de grande longueur d'onde (46) comporte une couche d'oxydation inférieure (28) d'AlGaAs, et

une première couche de contact (14) est disposée au-dessus de ladite couche d'oxydation supérieure (38) d'AlGaAs,

une seconde couche de contact (36) est intercalée entre la couche d'oxydation supérieure (38) d'AlGaAs et la couche d'oxydation inférieure (28) d'AlGaAs,

déposer un premier métal sur ladite première couche de contact (14) pour réaliser un premier contact du dispositif semi-conducteur,

graver un mesa (12) dans le VCSEL de courte longueur d'onde (44) vers le bas vers ladite seconde couche de contact, de manière à former un champ autour du mesa (12),

déposer un second métal dans le champ pour réaliser un second contact du dispositif semiconducteur,

réaliser un motif d'un ou plusieurs trous au-dessus du mesa (12) sous la forme d'un anneau non continu,

graver le ou les trous du motif à partir du haut du mesa (12) vers le bas à la fois à travers la couche d'oxydation supérieure (38) d'AlGaAs et la couche d'oxydation inférieure (28) d'AlGaAs, et

oxyder le ou les trous gravés en une étape unique, de manière à former une ouverture d'oxyde supérieure (18) dans le VCSEL de courte longueur d'onde (44) et une ouverture d'oxyde inférieure (30) dans le VCSEL de grande longueur d'onde (46),

dans lequel l'ouverture d'oxyde supérieure (18) et l'ouverture d'oxyde inférieure (30) sont colinéaires le long de l'axe vertical central (48).

10. Procédé selon la revendication 9, dans lequel :

chacune parmi la couche d'oxydation supérieure (38) et la couche d'oxydation inférieure (28) peut être oxydée de façon sélective par rapport aux couches épitaxiales environnantes.

11. Procédé selon la revendication 9 ou 10, dans lequel :

la gravure du mesa (12) dans le VCSEL de courte longueur d'onde (44) utilise une gravure sèche à base de plasma.

12. Procédé selon la revendication 9 ou 10, dans lequel ;

la gravure du mesa (12) dans le VCSEL de courte longueur d'onde (44) utilise une gravure chimique humide.

13. Procédé selon l'une quelconque des revendications 9 à 12, dans lequel :

le mesa gravé (12) comporte le premier métal sur la surface supérieure du VCSEL de courte longueur d'onde (44).

14. Procédé selon l'une quelconque des revendications 9 à 13, comprenant en outre l'étape consistant à :

réaliser un alliage du premier contact et du second contact en utilisant un procédé de recuit thermique rapide.

15. Procédé selon l'une quelconque des revendications précédentes, dans lequel :

la gravure des trous du motif, à la fois à travers la couche d'oxydation supérieure (38) et la couche d'oxydation inférieure (28), est effectuée en une étape unique.

16. Procédé selon l'une quelconque des revendications précédentes, comprenant en outre les étapes consistant à :

avant la formation de motif du ou des trous, effectuer un dépôt de SiNx sur le dispositif.

17. Procédé selon la revendication 16, comprenant en outre l'étape consistant à :

retirer le dépôt de SiNx,
effectuer un dépôt anti-réflexion de grande longueur d'onde au-dessus du dispositif,
réaliser un motif du dépôt anti-réflexion, et
graver le dépôt anti-réflexion pour ouvrir un accès au premier contact et au second contact,

18. Procédé selon l'une quelconque des revendications précédentes, dans lequel :

l'ouverture d'oxyde supérieure (18) et l'ouverture d'oxyde inférieure (30) imposent le mode optique du dispositif semiconducteur.

19. Procédé selon l'une quelconque des revendications 9 à 18, comprenant :

une gravure au-delà de la couche d'oxydation supérieure (38) et s'arrêtant dans la couche de contact (36).

20. Dispositif semiconducteur comprenant :

une ouverture d'oxyde supérieure (18) définie dans une couche d'oxydation supérieure (38) au-dessus d'une ouverture d'oxyde inférieure

(30) définie dans une couche d'oxydation inférieure (28),

dans lequel l'ouverture d'oxyde supérieure (18) et l'ouverture d'oxyde inférieure (30) sont colinéaires le long d'un axe vertical central (48),

un contact électrique vers une couche de contact (36) entre la couche d'oxydation supérieure (38) et la couche d'oxydation inférieure (28),

dans lequel l'ouverture d'oxyde supérieure (18) fait partie d'un laser à émission de surface à cavité verticale de courte longueur d'onde (VCSEL) (44),

l'ouverture d'oxyde inférieure (30) fait partie d'un VCSEL de grande longueur d'onde (46), et

le VCSEL de courte longueur d'onde (44) pompe optiquement le VCSEL de grande longueur d'onde (46).

21. Dispositif semiconducteur selon la revendication 20,
dans lequel le VCSEL de grande longueur d'onde (46) comporta :

un miroir inférieur (22),
une tranche de région active (24) fondue avec le miroir inférieur (22), et
une tranche miroir supérieure (26) fondue avec la région active (24).

22. Dispositif semiconducteur selon la revendication 20 ou 21, dans lequel :

le VCSEL de grande longueur d'onde (46) émet de la lumière laser ayant une longueur d'onde située dans une plage allant d'environ 1250 nm à environ 1650 nm.

23. Dispositif semiconducteur selon l'une quelconque des revendications 20 à 22, dans lequel :

l'ouverture d'oxyde supérieure (18) et l'ouverture d'oxyde inférieure (30) sont centrées chacune autour de l'axe vertical central (48) dans des plans respectifs qui sont tous deux perpendiculaires à l'axe vertical central (48).

24. Dispositif semiconducteur selon l'une quelconque des revendications 20 à 23, dans lequel :

le VCSEL de courte longueur d'onde (44) est pompé électriquement et comporte un miroir supérieur dopé p (42).

25. Dispositif semiconducteur selon la revendication 24, dans lequel :

le courant est limité à circuler dans un trajet de courant qui comporte le miroir supérieur (42), l'ouverture d'oxyde supérieure (18) et la couche de contact (36).

26. Dispositif semiconducteur selon l'une quelconque des revendications 20 à 25, dans lequel :

le VCSEL de courte longueur d'onde (44) émet de la lumière laser ayant une longueur d'onde située dans une plage allant d'environ 700 nm à environ 1050 nm.

27. Dispositif semiconducteur selon l'une quelconque des revendications 20 à 26, dans lequel :

l'énergie optique est guidée par l'ouverture d'oxyde supérieure (18) et l'ouverture d'oxyde inférieure (30).

28. Dispositif semiconducteur selon l'une quelconque des revendications 20 à 27, dans lequel :

la couche d'oxydation supérieure (38) et la couche d'oxydation inférieure (28) forment un guide d'indice de réfraction latéral.

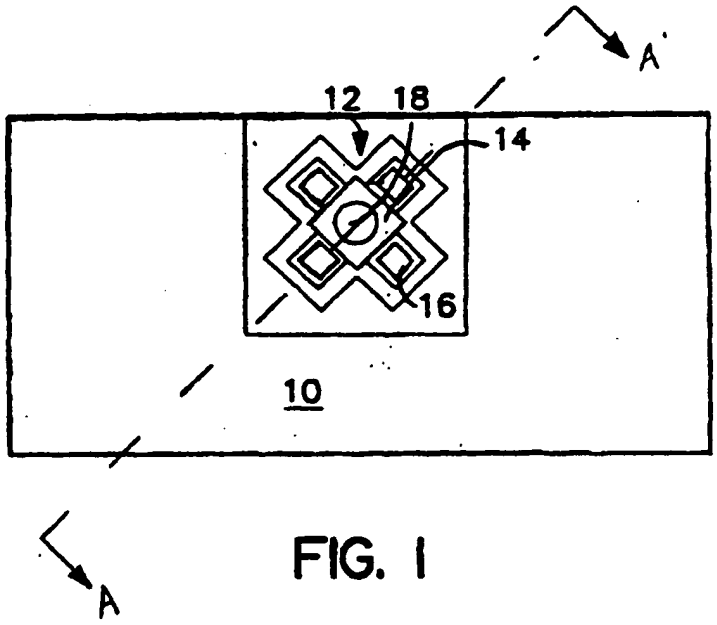

FIG. 1

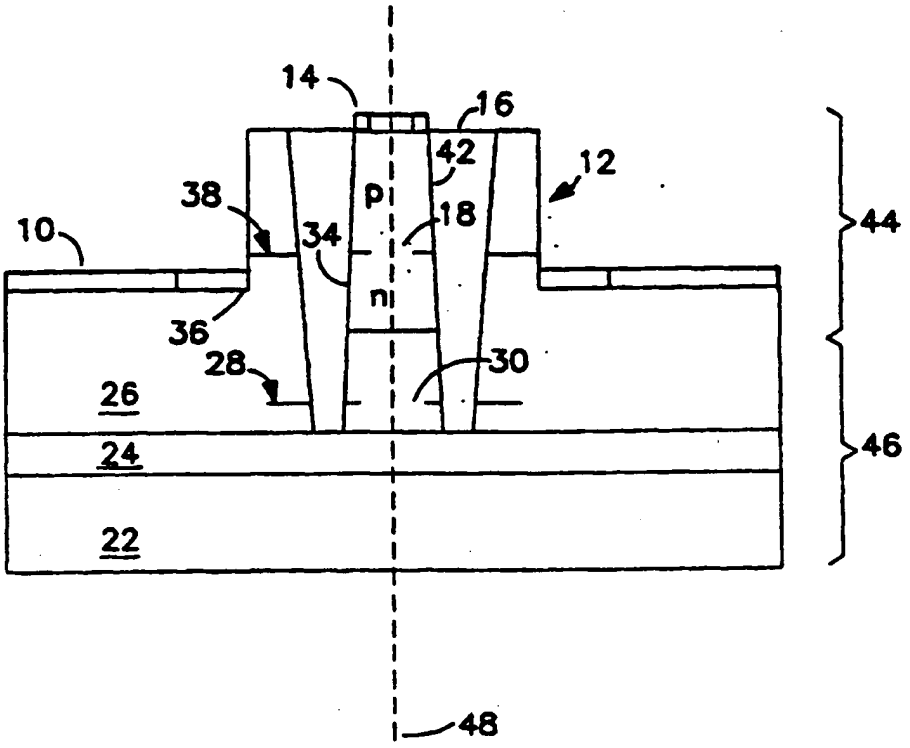

FIG. 2

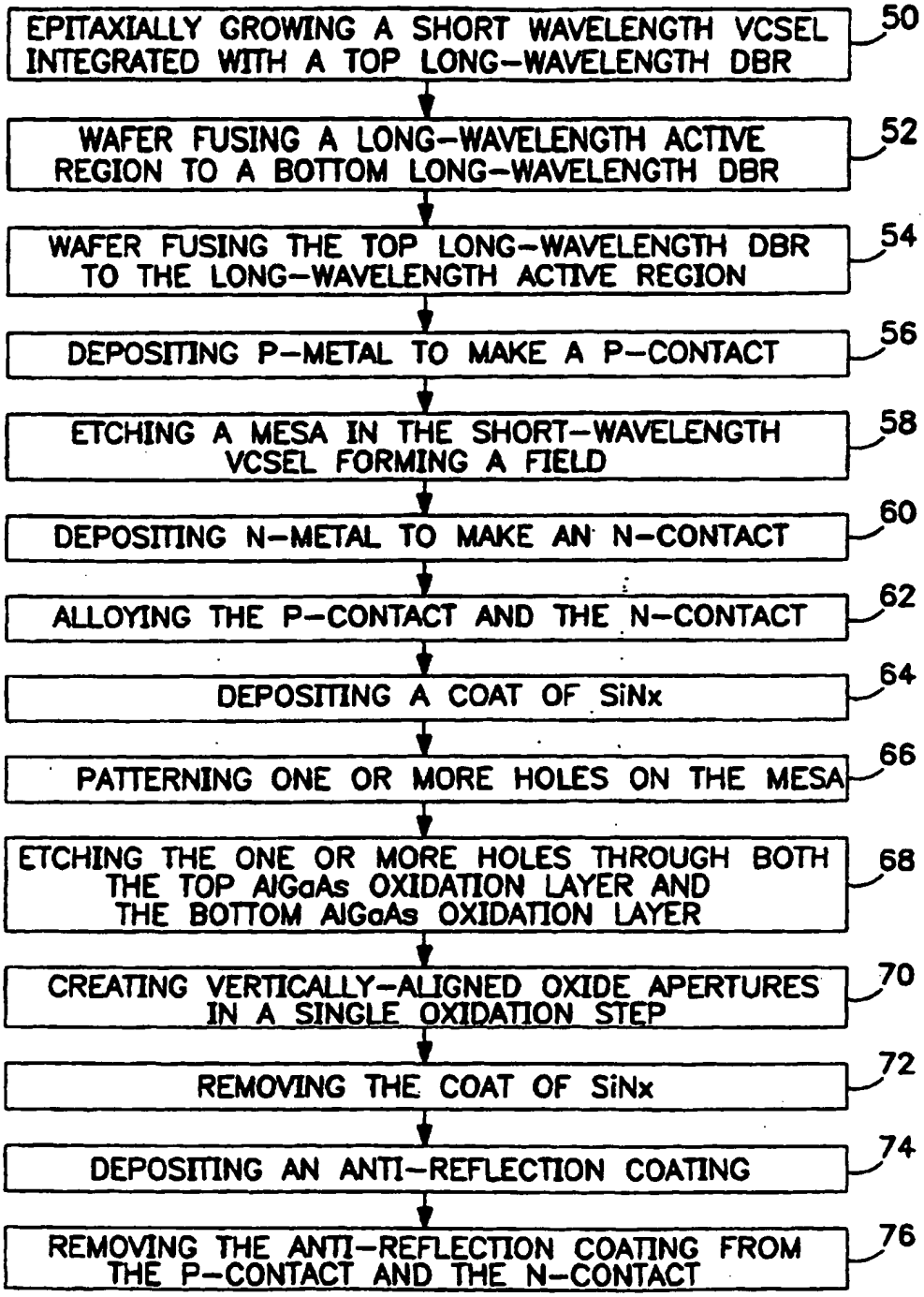
EPITAXIALLY GROWING A SHORT WAVELENGTH VCSEL INTEGRATED WITH A TOP LONG-WAVELENGTH DBR
50
WAFER FUSING A LONG-WAVELENGTH ACTIVE REGION TO A BOTTOM LONG-WAVELENGTH DBR
52
WAFER FUSING THE TOP LONG-WAVELENGTH DBR TO THE LONG-WAVELENGTH ACTIVE REGION
54
DEPOSITING P-METAL TO MAKE A P-CONTACT
56
ETCHING A MESA IN THE SHORT-WAVELENGTH VCSEL FORMING A FIELD
58
DEPOSITING N-METAL TO MAKE AN N-CONTACT
60
ALLOYING THE P-CONTACT AND THE N-CONTACT
62
DEPOSITING A COAT OF SiNx
64
PATTERNING ONE OR MORE HOLES ON THE MESA
66
ETCHING THE ONE OR MORE HOLES THROUGH BOTH THE TOP AlGaAs OXIDATION LAYER AND THE BOTTOM AlGaAs OXIDATION LAYER
68
CREATING VERTICALLY-ALIGNED OXIDE APERTURES IN A SINGLE OXIDATION STEP
70
REMOVING THE COAT OF SiNx
72
DEPOSITING AN ANTI-REFLECTION COATING
74
REMOVING THE ANTI-REFLECTION COATING FROM THE P-CONTACT AND THE N-CONTACT
76

FIG. 3